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# Antimonide-Based Compound Semiconductors for Low-Power Electronics

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**Abstract**—Quantum wells formed from antimonide-based compound semiconductors are exploited in n-channel field-effect transistors (FETs) operating at high speeds with ultra-low power consumption. Compressive strain enhances hole mobilities, making these materials strong candidates for p-channel FETs and complementary circuits. Recent work focuses on incorporation of gate oxides and integration of n- and p-channel FETs.

**Keywords**—FET, antimonide, CMOS, low-power

High-speed, low power high-electron mobility transistors (HEMTs) can be fabricated from InAs quantum wells clad by Al(Ga)Sb barriers [1]. Advantages of this material system include the high electron mobility (30,000 cm<sup>2</sup>/V-s at 300K) and velocity (4 x 10<sup>7</sup> cm/s) of InAs, and a large conduction band offset between InAs and Al(Ga)Sb. The large offset results in good carrier confinement and enhanced radiation tolerance. InAs HEMTs with 100-nm gate-length have exhibited unity-current-gain cutoff frequency,  $f_T$ , and unity-power-gain cutoff frequency,  $f_{max}$ , values of 200-300 GHz. Compared to state-of-the-art InP-based HEMTs with the same gate length, the InAs HEMTs provide equivalent high-speed performance at 5-10 times lower power dissipation. These transistors exhibit low microwave noise, with noise figures of 0.6-0.8 dB at 10 GHz [1]. Circuits based upon InAs HEMTs have been reported in the X-band, Ka-band, and W-band. For example, a three-stage W-band low-noise amplifier (LNA) was demonstrated with 11 dB gain at a total chip dissipation of only 1.8 mW at 94 GHz [2]. This is a factor of 3 lower power than comparable InP-based LNAs at the same frequency. In addition, antimonide-based semiconductors have been used to fabricate low-power heterojunction bipolar transistors [3], heterostructure barrier varactors for use as frequency multipliers [4], and p-n diodes for THz mixer applications [5].

Recently, there has been interest in the potential of III-V FETs for advanced logic applications which could enhance digital circuit functionality and extend Moore's law [6,7]. For these applications, a key to low power operation is the ability to make complementary circuits. In III-V materials, one challenge centers on maximizing the hole mobility in p-channel FETs. Strain and confinement can split the heavy- and light-hole valence bands, resulting in a predicted lower effective mass and higher mobility. We have demonstrated

this with compressively-strained In<sub>x</sub>Ga<sub>1-x</sub>Sb quantum wells clad by Al<sub>0.8</sub>Ga<sub>0.2</sub>Sb, and GaSb clad by AlAs<sub>y</sub>Sb<sub>1-y</sub> (see Fig. 1). In both systems, hole mobilities as high as 1500 cm<sup>2</sup>/V s were achieved at room temperature (a world record for any III-V compound), and p-channel FETs were demonstrated [8-10]. GaSb QWs on InP substrates reached record-low sheet resistivities of 1500  $\Omega/\square$  [11]. An Intel/Quintiq collaboration investigated p-FETs with InSb QWs and achieved an  $f_T$  of 140 GHz for a 40 nm gate length [12]. Modeling suggests that InGaSb p-FETs will have higher  $I_{ON}/I_{OFF}$  ratios than InSb p-FETs because of the smaller valence band offset for InSb QWs [13]. Application of uniaxial strain has also enhanced the performance of InGaSb-channel p-FETs [14].

An Sb-based CMOS requires deposition of high- $\kappa$  dielectric layers on semiconductors with low interface state densities. This has been demonstrated for n- and p-GaSb using HCl etching followed by atomic layer deposition (ALD) of Al<sub>2</sub>O<sub>3</sub> [15,16]. Recently, *in situ* hydrogen plasma cleaning was applied to GaSb prior to Al<sub>2</sub>O<sub>3</sub> deposition by ALD [17]. As shown in Fig. 2, the 100W plasma resulted in excellent Fermi level modulation, eliminating the need for chemical etching.

One strong candidate for the n-channel material in CMOS is InAsSb. MOSFETs with 150 nm gate length have an effective electron mobility of 6000 cm<sup>2</sup>/V s, an  $f_T$  of 120 GHz, and a source-side injection velocity of 2.7 x 10<sup>7</sup> cm/s [18]. These devices could be combined with p-InGaSb channel MOSFETs [19], with the advantage of similar lattice constants.

An alternative is to integrate Sb-based p-FETs and InP-based n-FETs, taking advantage of the maturity of InP n-FETs for analog applications. The 4% lattice mismatch between GaSb and InP could be tolerated if a buffer layer of AlGaAsSb ( $a_0 \sim 6.0$  Å) could be used with (In)GaSb p-channels in 2% compressive strain and InGaAs n-channels in 2% tensile strain (Fig. 1). The p-FETs were previously demonstrated [10,16]. As a step toward integration of the (In)GaSb-channel p-FETs with the InGaAs-channel n-FETs using the same buffer layer, we have demonstrated In<sub>x</sub>Ga<sub>1-x</sub>As/In<sub>0.52</sub>Al<sub>0.48</sub>As QWs ( $x = 0.64, 0.80$  and  $1.0$ ) on AlGaAsSb buffer layers (Fig. 3) with mobilities as high as 9000-11,000 cm<sup>2</sup>/V s for tensile strains up to 2%. The FET I-V characteristics for In<sub>0.64</sub>Ga<sub>0.36</sub>As are shown in Fig. 4. The best devices have a DC transconductance of 300 mS/mm, an  $f_T$  of 160 GHz, and an  $f_{max}$  of 150 GHz for a 90 nm gate length.

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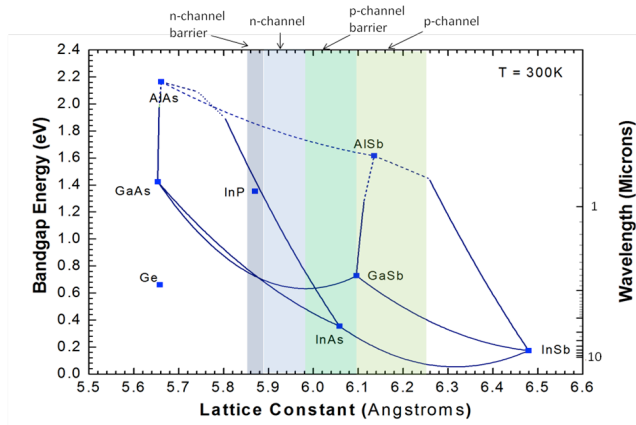


Figure 1: Energy gap vs. lattice constant indicating the typical parameters for n- and p-channel FETs.

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$\text{In}_x\text{Ga}_{1-x}\text{As}$ 2 nm
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ 4 nm
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ 5 nm <span style="color: #00AEEF;">Te <math>\delta</math> Doping <math>\uparrow</math></span>
$\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ 15 nm
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ 6 nm
$\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}/\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ digital superlattice ( $\sim 1.5 \mu\text{m}$ )
$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ 0.16 $\mu\text{m}$
InP substrate, S.I. (001)

Figure 3: Cross-section of InGaAs/InAlAs HEMT in tension. The sample was not rotated during the AlGaAsSb buffer layer, resulting in the lattice constant varying from 5.97 to 6.01 Å across the substrate.

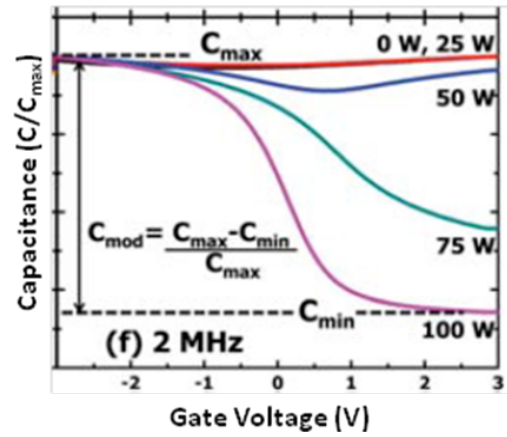


Figure 2: Normalized capacitance vs. gate voltage for GaSb MOS capacitors with different H plasma cleaning powers prior to ALD of  $\text{Al}_2\text{O}_3$  [17].

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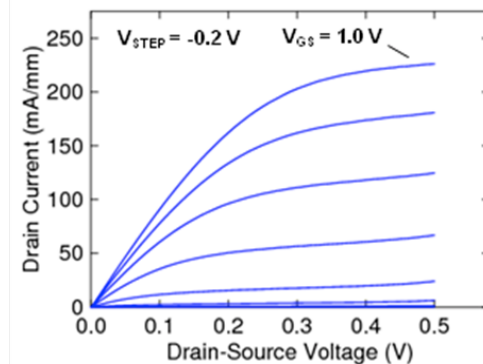


Figure 4: Drain characteristics for InGaAs-channel HEMT in tension with  $L_G = 100 \text{ nm}$  and  $W_G = 31 \mu\text{m}$ .